3/17/03
#11(KGT
Limo)
Appeal
Brief

TS99-656

Application No. 09/689,930

APPEAL BRIEF

TO: Commissioner of Patents and Trademarks
Washington, D.C. 20231

FROM: George O. Saile, Reg. No. 19,572
28 Davis Ave.
Poughkeepsie, N.Y. 12603

DATE: 28 February 2003

REF:

Applicant:	LIU, CHUNG-SHI ET AL.
Serial #:	09/689,930
Art Unit:	1756
File Date:	10/13/2000
Att'y No.:	TS99-656
Examiner:	SAGAR, KRIPA
Title:	NEW DUAL DAMASCENE PROCESS

Sir:

In response to rejection of the claims in the above referenced application for United States Patent in an office action mailed 04 September 2002 and made FINAL, applicants filed a notice of appeal on 04 December 2002. This is in response to the Advisory office action mailed on 26 November 2002. In accord with applicants' notice of appeal, please accept this brief. No oral hearing is requested.

The Commissioner of Patents and Trademarks is hereby authorized to charge the fee of $320.00 associated with this appeal brief to Deposit Account No. 19-0033, along with any additional extension fee required.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231 on March 7, 2003.

Signature ______ Date: 3/7/03
Stephen B. Ackerman, Reg. No. 37,761

03/12/2003 TTRAN1 00000065 190033 09689930
01 FC:1251 110.00 CH

03/12/2003 TTRAN1 00000065 190033 09689930
02 FC:1402 320.00 CH

APPEAL BRIEF

1. Real Party in Interest

The real party in interest for this application is the assignee:

Taiwan Semiconductor Manufacturing Ltd.
121 Park Ave. Rd. 3
Science-Based Industrial Park
Hsin-Chu, Taiwan
Republic of China

An assignment has been recorded for this United States Patent application.

2. Related Appeals and Interference's

There are no related appeals or interference's for this United States Patent application.

3. Status of the Claims:

Claims 1-30 remain in this application. Claims 1-30 have been finally rejected under 35 U.S.C. 103(a). No claims have been allowed.

4. Status of the Amendments:

An Amendment to the claims, reply mailed on 14 May 2002, (first response), was submitted after a first office action, mailed on 14 February 2002. This Amendment was entered. Another Amendment, reply mailed on 04 November 2002, (second response), was submitted after the office action made FINAL mailed on 04 September 2002, and will be entered for purposes of Appeal. Applicants filed a notice of appeal on 04 December

2002 for TS99-656, after an Advisory Action. This is in response to the advisory office action mailed on 26 November 2002.

5. <u>Summary of Invention</u>:

It is a general object of the Applicant's claimed invention to provide a new and improved method of forming semiconductor integrated circuit devices, and more specifically, for the formation of self-aligned dual damascene interconnects and vias. This non-obvious method incorporates two positive photoresist systems, which have different wavelength sensitivities, to form both via and trench openings with only a two-step etching process. In addition, the two layers of photoresist exhibit different etch resistant properties, for subsequent selective reactive ion etching steps. The use of a "high contrast" positive photoresist system has been developed wherein the resist system exposure sensitivity is optimized for wavelengths, deep-UV (248nm) for the top layer of resist, the trench pattern, and I-line (365nm) for the bottom layer of resist, the via pattern. The resist system provides a process in dual damascene for trench/via formation and has the following properties: selective etch resistance, thermal stability

during processing, ease of processing and developing, and good adhesion properties.

The main embodiments of the Applicant's claimed invention are found in independent Claim 1. Claim 1, lines 1-8, states:

"A method of photoresist processing comprising:

providing a substrate over which is formed composite layers of insulation comprising a first layer of dielectric separated from a second layer of dielectric by an intermediate etch stop layer of dielectric;

forming a top dielectric layer over said composite layers of dielectric;"

The Specifications describing the above are found on p. 14, line 6, first paragraph, of the Applicant's claimed invention, and refer to Fig. 1A, below:

"Referring to Fig. 1A, which in cross-sectional representation, shows a semiconductor silicon substrate 1 with an interlevel dielectric (ILD) layer 2 and with the first level of metal copper wiring 3 being defined, embedded in the a layer of insulator (not shown in Figs.). The first embodiment of the present invention starts with these layers in place. Next, a silicon nitride etch stop layer 4 is deposited on the metal copper wiring layer 3. Next, a low

dielectric constant layer 5 is deposited over the passivation layer 4. Another silicon nitride etch stop layer 6, an intermediate etch stop layer, is deposited in a thickness from approximately 200 to 500 Angstroms, over the first low dielectric constant layer 5. Another low dielectric constant layer 7 is deposited over the silicon nitride etch stop layer 6 and a passivating, top insulating layer, anti-reflective coating (ARC) of silicon oxynitride 8, thickness approximately 300 to 1000 Angstroms, is placed over the second low dielectric constant layer 7."

A key embodiment to the Applicant's claimed invention is the first photoresist layer and exposure of this photoresist for subsequent via formation, referring to Claim 1, lines 9-13, below:

"forming a first photoresist layer over said composite layers of insulation and top insulating layer;

patterning a via hole pattern in said first photoresist layer by exposing to I-line 365nm radiation and developing;"

The Specifications describing the above are found on p. 15, line 9, second paragraph, of the Applicant's claimed invention, and refer to Fig. 1A and Fig. 1B, below.

"Again referring to Fig. 1A, which in cross-sectional representation shows the first embodiment of this invention. Firstly, a layer of positive photoresist 9, which is sensitive to only I-line (365nm) radiation, termed PR1 for reference, is coated on top of the silicon oxynitride 8 layer. This layer of photoresist 9 is then exposed to I-line radiation 10 and developed using a mask 11 that patterns the contact via hole opening, in the exposed resist 12. Referring to Fig. 1B, which in cross-sectional representation shows the result of the first embodiment of this invention, the patterned photoresist 9 with contact via hole opening 13."

Another key embodiment to the Applicant's claimed invention is the second photoresist layer and exposure of this photoresist for subsequent trench formation, referring to Claim 1, lines 14-18, below:

"forming a second photoresist layer over via patterned said first photoresist layer;

patterning a trench line pattern in second photoresist layer by exposing to deep-UV 248nm radiation and developing;"

The Specifications describing the above are found on p. 15, line 4 from bottom, third paragraph, and also on p. 16, line 8, second paragraph, of the Applicant's claimed invention, and refer to Fig. 2A and Fig. 2B, below:

"Referring to Fig. 2A, which in cross-sectional representation shows the second embodiment of this invention. Another layer of photoresist positive resist 20, sensitive to deep-UV (248nm), termed PR2 for reference, is coated on top of the via patterned first layer of resist 9, termed PR1. This second layer of photoresist 20 is then exposed to deep-UV (23) and developed using a mask 21 that patterns the trench or line opening 22. This second resist process does not affect the exposed and developed bottom layer of resist 9, which is only sensitive to I-line (365nm) radiation.

Referring to Fig. 2B, which in cross-sectional representation shows the result of the second embodiment of this invention, the patterned photoresist 20 with trench or line opening 22 patterned. Thus, trench line pattern 22 and via hole pattern 13, patterned in the two layers of resist, are formed. These patterns in subsequent etch steps are transferred into the composite layers of insulation by a two-step, selective reactive ion etch process."

Yet another key embodiment to the Applicant's claimed invention are the etch steps that transfer the photoresist pattern of via and trench into the actual via and trench, in the composite layers of insulation, by a two-step, selective reactive ion etch process, referring to Claim 1, lines 14-30, below:

"etching top and second layer of dielectric underlying first layer of photoresist using the via hole pattern layer;

etching said intermediate layer of dielectric under said second layer of dielectric using the first layer of photoresist as a mask;

etching said composite layer of insulation transferring said trench line pattern into said first layer of photoresist and into said second layer of dielectric and transferring said via hole pattern into said intermediate layer of dielectric and into said first layer of dielectric;"

The Specifications describing the above are found on p. 17, line 10, second and third paragraph, of the Applicant's claimed invention, and refer to Fig. 3A and Fig. 3B, describing the etch processes, below:

"Referring to Figs. 3A - 3B, which in cross-sectional representation shows the final results of embodiments of the present invention. In Fig. 3A, the remaining photoresist

shown (9), is subsequently stripped away by ashing, as shown in Fig. 3B. As shown in Fig. 5B, thus is formed trench line opening 50 and via hole opening 52 for a dual damascene process. Note that in etching the trench and via openings, the photoresist also becomes partially consumed during the etching.

Referring to Fig. 3A, the resist patterns that were formed and shown in Fig. 2B, for trench and via, are transferred or replicated into the composite layers of insulation by a two-step, selective reactive ion etch process. Details of the two-step, selective reactive ion etch process are as follows. As shown in Fig. 3A, the following is a list of the various layers of insulator that are etched by this two-step, selective reactive ion etch process, etching down through: (8) the top SiON layer, the second layer of dielectric (7) underlying the first layer of photoresist (9), the intermediate layer of dielectric (6) under second layer of dielectric (7). Further, etching the composite layer of insulation transferring said trench line pattern into the first layer of photoresist (9) and into the second layer of dielectric (7) and transferring said via hole pattern into

the intermediate layer of dielectric (6) and into the first layer of dielectric (5)."

Final steps to the Applicant's claimed invention are the removal of photoresist and conventional filling of the formed trench and via openings with a dual damascene metal fill process, referring to Claim 1, lines 31-32, below:

"removing said layers of photoresist and filling the trench line and via hole openings with metal."

The Specifications describing the above are found on p. 19, line 1, first paragraph, of the Applicant's claimed invention, describing the photoresist strip and metal fill processes, below:

"After the photoresist layers are stripped away by ashing and any remaining etch stop material (4), which is SiN or SiC, is removed by a second step of etching (as shown in Fig. 3B). The dual damascene structure is now ready for subsequent metal fill, forming metal line and contact via hole interconnections on the semiconductor substrate . The subsequent dual damascene processing steps include: deposition of copper metal with removal of the excess copper by chemical mechanical polish (CMP), thus forming inlaid copper interconnects and contact vias."

6. Issues:

Whether or not Claims 1-7,9-17,19-27,29 and 30 are unpatentable under 35 U.S.C. 103(a) over Jang in view of Tobben and further in view of Orvek.

Whether or not Claims 8,18 and 28 are unpatentable under 35 U.S.C. 103(a) over Jang in view of Tobben and further in view of Orvek as applied to claims 1-7,9-17,19-27,29 and 30 above, and further in view of Pu.

7. Grouping of Claims:

Claims 1-30 are in a single group of Claims.

8.1 OPENING ARGUMENTS:

CLAIM REJECTIONS - 35 U.S.C. 103(a)

Prior art fails to disclose or suggest, the Applicant's non-obvious claimed invention that teaches the incorporation of two different positive photoresist systems, which have different wavelength sensitivities, to form via and trench openings with only a two-step etching process. In addition, the two layers of photoresist exhibit different etch resistant properties, for subsequent selective reactive ion etching steps. There are significant patentable differences

between the Applicant's claimed invention and the prior art references, as shown below.

8.2 ARGUMENTS:

Reconsideration of the rejection of claims 1-7, 9-17, 19-27,29,30 under 35 U.S.C. 103(a), as being unpatentable over Jang (US 6,110,648, hereafter referred to as Jang), in view of Tobben et al.(US 6,103,456, hereafter referred to as Tobben), and further in view of Orvek et al.(US 4,770,739, hereafter referred to as Orvek), is requested, based on the following.

There are significant patentable differences between the Applicant's claimed invention and the prior art references of Jang, in view of Tobben, and further in view of Orvek. Jang, in view of Tobben, and further in view of Orvek, fail to disclose or suggest the Applicant's non-obvious method of incorporating two different positive photoresist systems, which have different wavelength sensitivities, to form via and trench openings with only a two-step etching process, referring to Figs. 2A-2B and 3A-B. Prior art methods neither teach nor suggest the Applicant's claimed invention. The main focus of the Jang invention is as the title states, "METHOD OF ENCLOSING COPPER CONDUCTOR IN A DUAL DAMASCENE PROCESS." Jang teaches a method of enclosing copper conductors in a

protective material. Hence, Jang claims that the problems of corrosion and de-lamination through diffusion of copper are eliminated. The Applicant's claimed invention is directed toward simplifying a dual damascene process by saving processing steps, reducing etch steps, by the specific use of two different photo-resists. The Jang method, in view of Tobben, and further in view of Orvek, fail to disclose or suggest the Applicant's non-obvious method. In fact, the Jang method, for example, teaches a convention method of fabricating dual damascene openings by using two independent photoresist patterning multiple etching steps. In contrast, the Applicant's method teaches the use of two different photo-resists are used in the formation of self-aligned dual damascene interconnects and vias. Note, that the Applicant's claimed invention incorporates two positive photoresist systems, which have different wavelength sensitivities, to form trench and via openings with only a two-step etching process, instead of the conventional three etching steps, as exemplified by prior art.

Furthermore, the Applicants agree with the Examiner that Jang does not teach the use of:

A) a top insulating dielectric layer over a three-layer stack (ref. Applicant's claims 1,5,11,15,21,25)

B) the use of a near-UV (365nm) photoresist and a deep UV (268nm) photoresist, applied as a two layer resist system

and patentable differences from Orvek, since the Applicant claims a scheme for a two pattern transfer system, instead of Orvek's one.

(ref. Applicant's claims 1,6,7,11,16,17,21,26,27)

C) Furthermore, Jang does not teach the following key points, found in the Applicant's claimed invention: the formation of self-aligned dual damascene interconnects and vias, which incorporate two positive photoresist systems, which have different wavelength sensitivities, to form trench and via openings with only a two-step etching process. In addition, the two layers of photoresist exhibit different etch resistant properties, for subsequent selective reactive ion etching steps.

In addition, there are significant patentable differences between the Applicant's invention and the prior art references of Jang, in view of Tobben. Tobben's invention is focused on the prevention of photoresist poisoning caused by reactive gases from a silicon oxynitride layer, which is used as a dielectric anti-reflective coating (DARC) for a subsequent overlying photoresist layer. There are significant patentable differences between the Tobben disclosure and the Applicant's dual damascene process using two resist layers. Agree with the Examiner that Tobben teaches the prior-art of a dual damascene process, with the use of a top silicon

oxynitride layer. This element is common to many processes in use, including that of the Applicant's claimed invention.

In addition, there are more significant patentable differences amongst the Applicant's claimed invention and the prior art references of Jang, in view of Tobben, and furhter in view of Orvek. For example, the Orvek disclosure is concerned with planarizing an irregular surface with a first layer of planarizing photoresist, the bottom layer. The second layer of photoresist is coated over the first, and forms a top layer. Agree with the Examiner that the two resist have different sensitivities to UV light, and the top resist is exposed and patterned. The top resist pattern is then transferred exactly to the bottom resist pattern. As the Examiner states, the Orvek process teaches that the Orvek process scheme increases resolution. However, the Orvek scheme produces added processing steps and is costly, in that two photo-resists are used to define only one pattern. There are major patentable differences between the Orvek process and that of the Applicant's process. The Orvek process uses two different photo-resists to define only one pattern, whereas the Applicant's process uses two different photo-resists to define two patterns, in dual damascene the trench and via. Politely disagree with the Examiner that it would have been obvious to use a deep UV resist over a near-UV resist in Jang and Tobben's dual damascene process,

just because Orvek teaches an increase in resolution. The key point is that Orvek teaches an increase in resolution for defining or transferring only one image size pattern, which fails to disclose or suggest the Applicant's non-obvious method, as stated above.

The combination of the teaching of Jang, Tobben and Orvek still fail disclose or suggest the Applicant's claimed invention, as claimed in the Applicant's Claims 1-30.

Due to the above arguments, the Applicant's Claims 1-30, are believed to be patentable over Jang, Tobben and Orvek.

In conclusion, for state-of-the-art advanced applications in dual damascene technology, the Applicant's invention is believed to be patentable over Jang, Tobben, and Orvek, because there is insufficient basis for concluding that the modification of Prior Art disclosures would have been obvious to one skilled in the art. That is to say, there must be something in the Prior Art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination of Jang, Tobben, and Orvek.

Reconsideration of the rejection of claims 8,18,28 under 35 U.S.C. 103(a), as being unpatentable over Jang (US 6,110,648, hereafter referred to as Jang), in view of Tobben et al.(US 6,103,456, hereafter referred to as Tobben), and further in view of Orvek et al.(US 4,770,739, hereafter referred to as Orvek), as applied to claims 1-7, 9-17, 19-27, 29,30 above, and further in view of Pu et al.(US 5,843,847, hereafter referred to as Pu), is requested, based on the following.

There are significant patentable differences amongst the Applicant's invention and the prior art references of Jang, in view of Tobben, and further in view of Orvek, and further in view of Pu. Jang, in view of Tobben, and further in view of Orvek, and further in view of Pu, fail to disclose or suggest the Applicant's non-obvious method of incorporating two different positive photoresist systems, which have different wavelength sensitivities, to form via and trench openings with only a two-step etching process, referring to Figs. 2A-2B and 3A-B. Prior art methods neither teach nor suggest the Applicant's claimed invention. Specifically, referring to the Pu disclosure, as its title indicates, it is concerned with selective etching processes. It does not address the Applicant's claimed invention and Pu's figures indicate only one photoresist layer, reference Pu figures:

Fig. 1A, Fig. 1B, Fig. 1C, and Fig. 1D, in each the photoresist layer is labeled #40. Agree with the Examiner that some of the process chemistry for reactive ion etching of silicon nitride and silicon oxynitride, as taught by Pu and the Applicant's are similar, as the chemistries would be for etching nitride layers.

Politely disagree with the Examiner that, it would have been obvious to one of ordinary skill in the art at the time of the Applicant's claimed invention was made to:
(A) use Pu's process to etch the layers on, (B) Jang, and (C) Tobben's stack with, (D) Orvek's resists, because (E) Pu, teaches that this leads to better etch.

In addition, the Applicant's two layers of photoresist were especially formulated to exhibit different etch resistant properties, for subsequent selective reactive ion etching steps, for via and trench formation.

The combination of the teaching of Jang, Tobben, Orvek and Pu still fail to disclose or suggest the Applicant's claimed invention, as claimed in the Applicant's Claims 1-30, also referring to Fig. 2A and Fig. 2B.

8.2 <u>FINAL SUMMATION</u>:

Due to the above arguments, the claims are believed to be patentable over Jang, Tobben, Orvek and Pu.

Again, politely disagree with the Examiner that, it would have been obvious to one of ordinary skill in the art at the time of the Applicant's claimed invention was made to: (A) use Pu's process to etch the layers, on Jang (B), and on (C) Tobben's stack, with (D) Orvek's resists, because Pu (E), teaches that this leads to better etch (F). Going from point "A" to point "F", seems to be simply not "obvious".

In conclusion, for state-of-the-art advanced applications in dual damascene technology, the Applicant's claimed invention is believed to be patentable over Prior Art references Jang, Tobben, Orvek and Pu, because there seems to be insufficient basis for concluding that the modification of Prior Art disclosures would have been obvious to one skilled in the art. That is to say, there must be something in the Prior Art or line of reasoning to suggest that the combination of these various references is desirable. We believe that there is no such basis for the combination of Jang, Tobben, Orvek and Pu.

All specifications and claims are believed to be in allowable condition.

Applicants request that the Board of Appeals reverse the holding of the Examiner in finally rejecting the Claims in the application. Allowance of all the claims is requested.

Respectfully submitted,

Stephen B. Ackerman, Reg. No. 37,761

ADDENDUM

The Claims outstanding in this application for United States Patent are as follows:

1. A method of photoresist processing comprising:

providing a substrate over which is formed composite layers of insulation comprising a first layer of dielectric separated from a second layer of dielectric by an intermediate etch stop layer of dielectric;

forming a top dielectric layer over said composite layers of dielectric;

forming a first photoresist layer over said composite layers of insulation and top insulating layer;

patterning a via hole pattern in said first photoresist layer by exposing to I-line 365nm radiation and developing;

forming a second photoresist layer over via patterned said first photoresist layer;

patterning a trench line pattern in second photoresist layer by exposing to deep-UV 248nm radiation and developing;

etching top and second layer of dielectric underlying first layer of photoresist using the via hole pattern layer;

etching said intermediate layer of dielectric under said second layer of dielectric using the first layer of photoresist as a mask;

etching said composite layer of insulation transferring said trench line pattern into said first layer of photoresist and into said second layer of

dielectric and transferring said via hole pattern into said intermediate layer of dielectric and into said first layer of dielectric;

removing said layers of photoresist and filling the trench line and via hole openings with metal.

2. The method of claim 1, wherein said substrate is semiconductor single crystal silicon or an IC module.

3. The method of claim 1, wherein said composite layers of insulation are low dielectric constant dielectric material consisting of $SiOF_x$, $SiOC_x$, $SiOH_x$, where the value of "x" is in range from 0.5 to 1.0, in a thickness range from approximately 4000 to 12000 Angstroms for said first layer of dielectric and in a thickness range from approximately 4000 to 8000 Angstroms for said second layer of dielectric.

4. The method of claim 1, wherein said intermediate etch stop layer of dielectric consists of silicon nitride, Si_xN_y, where the value of "x" is in range from 2 to 3 and the value of "y" is in a range from 3 to 4, in a thickness range from approximately 200 to 500 Angstroms, and can used in tandem with another etch stop layer or without said etch stop.

5. The method of claim 1, wherein said top insulating layer is silicon oxynitride, SiON, in a thickness from approximately 300 to 1000 Angstroms.

6. The method of claim 1, wherein said first photoresist layer is positive photoresist consisting of I-line positive resists, in a thickness range from approximately 6000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light I-line radiation of wavelength 365nm.

7. The method of claim 1, wherein said second photoresist layer is positive photoresist consisting of positive DUV, 248nm photoresist, in a thickness range from approximately 5000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light deep-UV radiation of wavelength 248nm.

8. The method of claim 1, wherein said etching is performed in a two-step etch , selective reactive ion etch, RIE, with the first step process chemistry, for etching SiON and SiN: CHF_3, C_2F_6, N_2 O_2 Ar, between 500 to 1200 Watts power, producing etch removal rates of between 1000 to 5000 Angstroms per minute, next applying: CO, C_4F_8, C_2F_6, Ar; the second step of etching to removing any SiN in the via: CF_4, Ar O_2, CH_3F,

between from 200 to 300 Watts power, producing etch rates from 1000 to 2000 Angstroms per minute, thus both the trench and via openings are formed in a dual damascene process.

9. The method of claim 1, wherein the dual damascene trench and via is lined with a diffusion barrier, filled with conducting metal and whereby the excess metal is removed by chemical mechanical polish.

10. The method of claim 1, wherein multilevel conducting layers are fabricated by repeating the process steps described in the method of claim 1.

11. A method of dual damascene patterning by use of two-layered photoresist process, having different wavelength sensitivities for each layer, comprising:

providing a substrate over which is formed composite layers of insulation wherein said composite layers comprise a first layer of dielectric separated from a second layer of dielectric by an intermediate etch stop layer of dielectric and etch stop layer of dielectric below the first layer of dielectric;

forming a top dielectric layer over said composite layers of dielectric;

forming a first photoresist layer over said composite layers of insulation and said top dielectric layer;

patterning a via hole pattern in said first photoresist layer composed by exposing to I-line 365nm radiation and developing said first photoresist layer by using a via hole mask;

forming a second photoresist layer over said first photoresist layer;

patterning a trench line pattern in said second photoresist layer by exposing to deep-UV 248nm radiation and developing said second photoresist layer by using a trench line mask;

etching, in two-step process, said second layer of dielectric underlying said first layer of photoresist using the via hole patterned layer of the first photoresist as a mask and transferring said via hole pattern into said second layer of dielectric;

etching said intermediate layer of dielectric under said second layer of dielectric using the first layer of photoresist as a mask and transferring said via hole pattern in said layer of photoresist into said intermediate layer of dielectric;

etching said composite layer of insulation transferring said trench line pattern into said first layer of photoresist and into said second layer of

dielectric to form a trench line opening, and at the same time transferring said via hole pattern into said intermediate layer of dielectric and into said first layer of dielectric to form a via hole opening;

removing said layers of photoresist and any exposed insulating material in the trench line opening and via hole opening;

depositing metal into the trench line and via hole opening with subsequent removal of excess metal by chemical mechanical polishing back, to form inlaid conducting interconnects lines and contact vias, in a dual damascene process.

12. The method of claim 11, wherein said substrate is semiconductor single crystal silicon or an IC module.

13. The method of claim 11, wherein said composite layers of insulation are low dielectric constant dielectric material consisting of $SiOF_x$, $SiOC_x$, $SiOH_x$, where the value of "x" is in range from 0.5 to 1.0, in a thickness range from approximately 4000 to 12000 Angstroms for said first layer of dielectric and in a thickness range from approximately 4000 to 8000 Angstroms for said second layer of dielectric.

14. The method of claim 11, wherein said intermediate etch stop layer of dielectric consists of silicon nitride, Si_xN_y, where the value of "x" is in range from 2 to 3 and the value of "y" is in a range from 3 to 4, in a thickness range from approximately 200 to 500 Angstroms, and can used in tandem with another etch stop layer or without said etch stop.

15. The method of claim 11, wherein said top insulating layer is silicon oxynitride, SiON, in a thickness from approximately 300 to 1000 Angstroms.

16. The method of claim 11, wherein said first photoresist layer is positive photoresist consisting of I-line positive resists, in a thickness range from approximately 6000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light I-line radiation of wavelength 365nm.

17. The method of claim 11, wherein said second photoresist layer is positive photoresist consisting of positive DUV, 248nm photoresist, in a thickness range from approximately 5000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light deep-UV radiation of wavelength 248nm.

18. The method of claim 11, wherein said etching is performed in a two-step etch , selective reactive ion etch, RIE, with the first step process chemistry, for etching SiON and SiN: CHF_3, C_2F_6, N_2 O_2 Ar, between 500 to 1200 Watts power, producing etch removal rates of between 1000 to 5000 Angstroms per minute, next applying: CO, C_4F_8, C_2F_6, Ar; the second step of etching to removing any SiN in the via: CF_4, Ar O_2, CH_3F, between from 200 to 300 Watts power, producing etch rates from 1000 to 2000 Angstroms per minute, thus both the trench and via openings are formed in a dual damascene process.

19. The method of claim 11, wherein the dual damascene trench and via is lined with a diffusion barrier, filled with conducting metal and whereby the excess metal is removed by chemical mechanical polish.

20. The method of claim 11, wherein multilevel conducting layers are fabricated by repeating the process steps described in the method of claim 11.

21. A method of dual damascene patterning by use of two-layered photoresist process, having different wavelength sensitivities for each layer, comprising:

providing a substrate over which is formed composite layers of insulation wherein said composite layers comprise a first layer of dielectric separated from a second layer of dielectric by an intermediate etch stop layer of dielectric and etch stop layer of dielectric below the first layer of dielectric;

forming a top dielectric layer over said composite layers of dielectric;

forming a first photoresist layer composed of polymer over said composite layers of insulation and said top dielectric layer;

patterning a via hole pattern in said first photoresist layer composed of polymer, positive type, by exposing to I-line 365nm radiation and developing said first photoresist layer by using a via hole mask;

forming a second photoresist layer composed of polymer over said first photoresist layer;

patterning a trench line pattern in said second photoresist layer composed of, polymer, positive type, by exposing to deep-UV 248nm radiation and developing said second photoresist layer by using a trench line mask;

etching in the first of a two-step selective reactive ion etch process using the following gases, for step one:

CHF_3, C_2F_6, N_2 O_2 Ar / CO, C_4F_8, C_2F_6, Ar, producing trench and via openings;

etching in the second of a two-step selective reactive ion etch process using the following gases, for step two:

CF_4, Ar O_2, CH_3F, removing SiN for bottom of via opening;

etching said second layer of dielectric underlying the first layer of photoresist using the via hole patterned layer of the first photoresist as a mask and transferring said via hole pattern into said second layer of dielectric, by etch step one above ;

etching said intermediate layer of dielectric under said second layer of dielectric using the first layer of photoresist as a mask and transferring said via hole pattern in said layer of photoresist into said intermediate layer of dielectric, by etch step one above;

etching said composite layer of insulation transferring said trench line pattern into said first layer of photoresist and into said second layer of dielectric to form a trench line opening, and at the same time transferring said via hole pattern into said intermediate layer of dielectric and into said first layer of dielectric to form a via hole opening, by etch step one above;

removing said layers of photoresist and any exposed insulating material in the trench line opening and via hole opening by ashing and by etch step two above;

depositing metal into the trench line and via hole opening with subsequent removal of excess metal by chemical mechanical polishing back, to form inlaid conducting interconnects lines and contact vias, in a dual damascene process.

22. The method of claim 21, wherein said substrate is semiconductor single crystal silicon or an IC module.

23. The method of claim 21, wherein said composite layers of insulation are low dielectric constant dielectric material consisting of $SiOF_x$, $SiOC_x$, $SiOH_x$, where the value of "x" is in range from 0.5 to 1.0, in a thickness range from approximately 4000 to 12000 Angstroms for said first layer of dielectric and in a thickness range from approximately 4000 to 8000 Angstroms for said second layer of dielectric.

24. The method of claim 21, wherein said intermediate etch stop layer of dielectric consists of silicon nitride, Si_xN_y, where the value of "x" is in range from 2 to 3 and the value of "y" is in a range from 3 to 4, in a thickness range from approximately 200

to 500 Angstroms, and can used in tandem with another etch stop layer or without said etch stop.

25. The method of claim 21, wherein said top insulating layer is silicon oxynitride, SiON, in a thickness from approximately 300 to 1000 Angstroms.

26. The method of claim 21, wherein said first photoresist layer is positive photoresist consisting of I-line positive resists, in a thickness range from approximately 6000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light I-line radiation of wavelength 365nm.

27. The method of claim 21, wherein said second photoresist layer is positive photoresist consisting of positive DUV, 248nm photoresist, in a thickness range from approximately 5000 to 10000 Angstroms and is selectively sensitive to and exposed to ultraviolet light deep-UV radiation of wavelength 248nm.

28. The method of claim 21, wherein said etching is performed in a two-step etch , selective reactive ion etch, RIE, with the first step process chemistry, for etching SiON and SiN: CHF_3, C_2F_6, N_2 O_2 Ar, between 500 to 1200 Watts power, producing etch removal rates of

between 1000 to 5000 Angstroms per minute, next applying: CO, C_4F_8, C_2F_6, Ar; the second step of etching to removing any SiN in the via: CF_4, Ar O_2, CH_3F, between from 200 to 300 Watts power, producing etch rates from 1000 to 2000 Angstroms per minute, thus both the trench and via openings are formed in a dual damascene process.

29. The method of claim 21, wherein the dual damascene trench and via is lined with a diffusion barrier, filled with conducting metal and whereby the excess metal is removed by chemical mechanical polish.

30. The method of claim 21, wherein multilevel conducting layers are fabricated by repeating the process steps described in the method of claim 21.